Notice of Allowability	Application No.	Applicant(s)	
	09/618,971	GUPTA, VIKRAM	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *February 2, 2005*.

2. ☒ The allowed claim(s) is/are *1-19 and 31-43*.

3. ☒ The drawings filed on *23 May 2004 and 02 February 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's communication dated February 2, 2005. Claims 1-19 and 31-43 of the application are pending.

Drawings

2. The drawing submitted for Figure 3 on February 2, 2005 is accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Matthew Zigmant on March 29, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. In the Claims:

In Claim 1, Lines 4-6, "providing an emulation circuit, which is capable of generating noise, and which has a configuration capable of being modified;

affixing said emulation circuit on a test substrate;"

has been changed to

-- providing a digital emulation circuit, which is capable of generating noise, and which has a configuration capable of being modified;

affixing said digital emulation circuit on a test substrate;--.

In Claim 1, Lines 12-13, "providing the digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the emulation circuit"

has been changed to

-- providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit --.

In Claim 3, Lines 3-5, "repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step"

has been changed to

-- repeating said affixing digital emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step --.

In Claim 19, Lines 1-2, "The method of claim 1, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion."

has been changed to

-- The method of claim 1, wherein a number of gates in said digital emulation circuit is substantially equivalent to a number of gates in said digital circuit portion.--.

In Claim 31, Lines 4-6, "providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic circuits;

affixing said emulation circuit on said integrated circuit;"

has been changed to

-- providing a digital emulation circuit, which is capable of generating noise, and which comprises a plurality of logic circuits;

affixing said digital emulation circuit on said integrated circuit;--.

In Claim 31, Lines 10-12, "testing said analog circuit version;

providing said digital circuit portion, wherein said digital circuit portion may be formed by rewiring said emulation circuit"

has been changed to

-- testing said analog circuit version while modifying the configuration of the digital emulation circuit; and

providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit, wherein said digital circuit portion is formed by rewiring said digital emulation circuit.--.

In Claim 33, Lines 3-5, "repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step"

has been changed to

-- repeating said affixing digital emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step --.

In Claim 35, Lines 1-2, "The method of claim 31, wherein said noise generated by said emulation circuit is substantially equivalent to noise generated by said digital circuit portion"

has been changed to

-- The method of claim 31, wherein said noise generated by said digital emulation circuit is substantially equivalent to noise generated by said digital circuit portion --.

In Claim 36, Lines 3-4, "providing an emulation circuit, which generates noise, and which comprises a circuit path that may be modified;"

has been changed to

-- providing a digital emulation circuit, which generates noise, and which comprises a circuit path that may be modified;--.

In Claim 36, Lines 9-12, "testing said analog circuit version, while modifying the circuit path in the emulation circuit; and

providing the digital portion, the digital portion having a configuration based on the testing of the analog circuit while modifying the circuit path in the emulation circuit"

has been changed to

-- testing said analog circuit version, while modifying the circuit path in the digital emulation circuit; and

providing the complete digital portion, the complete digital portion having a configuration based on the testing of the analog circuit while modifying the circuit path in the digital emulation circuit--.

In Claim 38, Lines 3-5, "repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step"

has been changed to

-- repeating said affixing digital emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step --.

In Claim 40, Lines 1-2, "The integrated circuit of claim 36 wherein said emulation circuit has at least one array comprising at least one shift register"

has been changed to

-- The integrated circuit of claim 36 wherein said digital emulation circuit has at least one array comprising at least one shift register --.

In Claim 43, Lines 1-3, "The integrated circuit of claim 36, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion"

has been changed to

-- The integrated circuit of claim 36, wherein a number of gates in said digital emulation circuit is substantially equivalent to a number of gates in said digital circuit portion --.

Reasons for Allowance

5. Claims 1-19 and 31-43 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a user programmable integrated circuit that includes on the same silicon die a set of programmable logic cells, a set of programmable mixed signal and analog cells, a microprocessor used for controlling and configuring the whole system and for running the general purpose programs and interfaces between the three; the configuration allows the programmable device to change the configuration fast; the system includes an emulator that links the user circuit entered in HDL with the hardware/software co-emulation and simulation engines; it is possible to co-emulate hardware and mixed signal applications in real time over the single silicon chip (**Insenser Farre et al.,** U.S. Patent 6,460,172);

(2) an apparatus and a method for generating noise representative of digital switching noise for use in evaluation and testing of analog and digital circuit; the generated noise is applied for evaluation of any possible performance degradation of analog or mixed-signal integrated circuit to help determine the need for effective noise suppression techniques and design modification of the circuit; the noise generating circuit is fabricated on a substrate and generates noise representative of the digital switching noise; the substrate is adaptable for fabricating the analog circuit on the substrate; the noise generator is programmable (**Boerstler et al,** U.S. Patent 5,668,507); and

(3) a mixed signal circuit including analog circuitry and digital circuitry partitioned from the analog circuitry and a boundary scan chain connected along the boundary between the analog and digital circuitry for selectively decoupling the analog from the digital circuitry during testing; the boundary scan chain cells are connected, so each cell can intercept a different one of the signals to be exchanged between the analog and digital circuitry; the apparatus simplifies the

testing of either analog or digital circuitry alone where the analog and digital circuitry are embedded in a single larger circuit (**Qureshi,** U.S. Patent 5,793,778).

6.1 Applicant's first set of claims consists of Claims 1-19.

Independent Claim 1 is directed to a method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions. The claim identifies the uniquely distinct features of:

"providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit".

Because the closest prior art fails to teach or fairly suggest providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit, as claimed by the Applicant, Claims 1-19 are deemed novel and allowable.

6.2 Applicant's second set of claims consists of Claims 31-35.

Independent Claim 31 is directed to a method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions. The claim identifies the uniquely distinct features of:

"providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit, wherein said digital circuit portion is formed by rewiring said digital emulation circuit".

Because the closest prior art fails to teach or fairly suggest providing the complete digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the digital emulation circuit, wherein said digital circuit portion is formed by rewiring said digital emulation circuit, as claimed by the Applicant, Claims 31-35 are deemed novel and allowable.

6.3 Applicant's third set of claims consists of Claims 36-43.

Independent Claim 36 is directed to an integrated circuit having digital and analog portions. The claim identifies the uniquely distinct features of:

"providing the complete digital portion, the complete digital portion having a configuration based on the testing of the analog circuit while modifying the circuit path in the digital emulation circuit".

Because the closest prior art fails to teach or fairly suggest providing the complete digital portion, the complete digital portion having a configuration based on the testing of the analog circuit while modifying the circuit path in the digital emulation circuit, as claimed by the Applicant, Claims 36-43 are deemed novel and allowable.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
March 29, 2005